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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,284	12/08/2005	Rainer Nase	0740-73	6250
616	7590	10/18/2007		
THE MAXHAM FIRM 9330 SCRANTON ROAD, SUITE 350 SAN DIEGO, CA 92121			EXAMINER PATEL, KAUSHIKKUMAR M	
			ART UNIT	PAPER NUMBER
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 10/541,284	Applicant(s) NASE, RAINER	
	Examiner Kaushikkumar Patel	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 July 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date <u>6/20/2006</u> | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Priority***

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Information Disclosure Statement***

2. The information disclosure statement (IDS) submitted on June 20, 2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has considered by the examiner.

### ***Drawings***

3. The drawings are not of sufficient quality to permit examination. Accordingly, replacement drawing sheets in compliance with 37 CFR 1.121(d) is required in reply to this Office action. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action.

### ***Claim Objections***

4. Claims 1 and 10 are objected to because of the following informalities:  
Claims 1 and 10 ends with " ; " but the claims must end with full stop (.), please make appropriate corrections.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 5, 6, 10, 11, 13 and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Sassa (US 6,098,077).

As per claim 1, Sassa teaches a method for memory management in smart card controllers or similar restricted hardware environment by writing of data into a data space in a persistent memory (col. 1, lines 6-10), said method comprising steps of:

a) splitting the persistent memory into blocks with fixed data length having logical block numbers (LBN) (col. 1, lines 35-41, col. 9, lines 10-18);

b) selecting the size of blocks as such that it is equal to--or equivalent to an integer ratio of--the length of a page in EEPROM to the physical size of the pages of the EEPROM memory existing on the card (col. 6, lines 25-30);

c) providing a Block Allocation Table (BAT) in order to calculate the physical place of the block in memory from the logical block number (col. 6, lines 32-39, col. 9, lines 10-20).

As per claim 5, Sassa teaches the method according to claim 1, wherein a linkage between blocks by writing the LBN of the following block to the header of the leading block is provided (col. 6, line 39 – col. 7, line 5).

As per claim 6, Sassa teaches the method according to 1, wherein a secure write mechanism is accomplished by replacing individual memory blocks by each other (col. 7, lines 11-25).

As per claim 10, Sassa teaches a device with a persistent memory and a block structure comprising (figs. 2 and 3):

- a) a memory managing system using a block oriented memory structure (fig. 3);
- b) blocks with the same, length and identifying them by their logical block number (LBN) (col. 1, lines 35-41, col. 9, lines 10-18);
- c) a block allocation table (BAT) to resolve the logical block number to a physical block number (PBN) and its physical address (col. 9, lines 10-20).

As per claim 11, Sassa teaches a device according to claim 10, further comprising a linkage between blocks by writing the LBN of the following block to the header of the leading one (col. 6, line 39 – col. 7, line 5).

As per claim 13, Sassa teaches a device according to claim 10 characterized in that the BAT is held in persistent memory (EEPROM) (col. 9, lines 40-41, col. 10, lines 8-10).

As per claim 14, Sassa teaches a device according to claim 10 characterized in that the BAT is held in non-persistent memory (RAM-BAT) and re-initialized on startup (col. 9, lines 39-40).

7. Claims 1-4, 10 and 12 are rejected under **35 U.S.C. 102(e)** as being anticipated by Gonzalez et al. (US 6,684,289).

As per claim 1, Gonzalez teaches a method for memory management in smart card controllers or similar restricted hardware environment by writing of data into a data space in a persistent memory (col. 1, lines 9-12), said method comprising steps of:

a) splitting the persistent memory into blocks with fixed data length having logical block numbers (LBN) (col. 5, line 47 – col. 6, line 27);

b) selecting the size of blocks as such that it is equal to--or equivalent to an integer ratio of--the length of a page in EEPROM to the physical size of the pages of the EEPROM memory existing on the card (col. 5, line 47 – col. 6, line 27, col. 7, lines 22-24);

c) providing a Block Allocation Table (BAT) in order to calculate the physical place of the block in memory from the logical block number (fig. 11, col. 10, lines 35-65).

As per claim 2, Gonzalez teaches the method according to claim 1, including the step of splitting a whole block into individual segments, whereby each fragment is belonging to a different data object (see abstract, figs. 6A, 6B, 8, col. 3, lines 4-10).

As per claim 3, Gonzalez teaches the method according to claim 2, including the step of identifying a corresponding segment through the block number of the whole

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block and the number of the individual segment (figs. 6A, 6B, 8, 9, 10, 11, col. 7, line 30 – col. 8, line 25).

As per claim 4, Gonzalez teaches the method according to claim 2, including defining a block header in the block with a list of entries providing information to localize the segments as well as defining their length (figs. 6A, 6B, 8, 9, 10, 11, col. 3, lines 4-10; col. 7, line 30 – col. 8, line 25).

Claims 10 and 12 are also rejected under same rationales as applied to claims 1-4 above.

### ***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sassa (US 6,098,077) as applied to claim 1 above, and further in view of Peterman (US 5,623,654) (submitted as an IDS).

As per claim 7, Sassa teaches all the limitations of claim 1 as above, but fails to teach blocks organized in form of ring list. Peterman teaches free blocks forming a ring list (Peterman, fig. 5, and col. 4, lines 37-49). It would have been obvious to one having ordinary skill in the art at the time of the invention to use ring list as taught by Peterman

in the system of Sassa to access free space quickly and efficiently (Peterman, col. 2, lines 29-39).

10. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sassa (US 6,098,077) as applied to claim 1 above, and further in view of Lasser (US 6,883,114).

As per claim 8, Sassa teaches all the limitations of claim 1 above, but fails to teach block header with a commit bit. Lasser teaches a use of commit bit (Lasser, figs. 5, 6A-6E, col. 9, line 3 – col. 10, line 62). It would have been obvious to one having ordinary skill in the art at the time of the invention to use commit bit as taught by Lasser in the system of Sassa to provide consistent data storage (Lasser, col. 2, lines 35-51).

As per claim 9, Lasser teaches toggling of a bit in commit block toggles the validity of the corresponding memory block (Lasser, col. 9, line 3 – col. 10, line 62, the “R” setting “1” or “0” or vice versa).

### ***Conclusion***

11. The examiner also requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line no(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.



12. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections See 37 CFR 1.111(c).

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Estakhri et al. (US 2001/0029564) teaches method of managing flash memory blocks using block allocation table with various flags to indicate old or new data.

Conley (US 6,763,424) teaches method of updating pages of non-volatile memory using flags.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.


If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

  
kmp

Kaushikkumar Patel  
Examiner  
Art Unit 2188

  
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SUPERVISORY PATENT EXAMINER  
10/15/07